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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,267	01/20/2004	Geum-Jin Yun	2557-000206/US	6863

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EXAMINER	
PATEL, PARESH H	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,267	YUN ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *28 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-27 in the reply filed on 04/01/2005 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-3 recites the limitation "the semiconductor device" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Objections

4. Claims 2-3 are objected to because of the following informalities: The semiconductor device should read multi-chip package and in claim 3 chip should be chips. Appropriate correction is required.

5. To expedite the prosecution the above change is assumed for examination of these claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, 8-10, 12-13, 21-24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Takizawa (US 6198663).

Regarding claims 1-5, 12 and 21,Takizawa discloses an integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package [60] formed of multiple types of semiconductor device (package) performs memory function; and

testing [using 70] the multi-chip package with an integrated burn-in test program [for different temperature and monitoring, see fig. 3A].

Regarding claims 8 and 22,Takizawa discloses the testing includes applying a specific test condition [see fig. 3A] during testing of each semiconductor device [see lines 44-47 and 59-63 of column 6], wherein the specific test condition is defined by a multiplexer selection function [using 71 of 70].

Regarding claims 9 and 23,Takizawa discloses the testing includes blocking some I/O terminals during testing of some semiconductor devices, wherein the blocking is defined by an I/O masking function [using 61a of 70].

Regarding claims 10 and 24,Takizawa discloses the testing includes setting a specific burn-in temperature condition for different types of semiconductor devices [see lines 44-47 and 59-63 of column 6].

Regarding claim 6, Takizawa in fig. 6 discloses burn-in board and chamber of burn-in equipment.

Regarding claims 13 and 26 Takizawa discloses bin sorting once for all different types of semiconductor devices of the multi-chip package based on the testing result [lines 31-35 of column 6].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 14-18, 20 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa in view of Goins, III (US 5931311).

Regarding claims 14-18, 20 and 27, Takizawa discloses an integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package [60] formed of multiple types of semiconductor device;

testing [using 70] the multi-chip package with an integrated burn-in test program (monitoring), including

blocking some I/O terminals [using 61a of 70] during testing of some semiconductor devices, wherein the blocking is defined by an I/O masking function,

setting a specific burn-in temperature condition for different types of semiconductor devices [see lines 44-47 and 59-63 of column 6], and

conducting a burn-in test [using 71 of 70] for the multiple types of semiconductor devices by applying a specific test condition [see lines 44-47 and 59-63 of column 6] for each semiconductor device, wherein the specific test condition is defined by a multiplexer selection function [using 71 of 70];

bin sorting once for all different types of semiconductor devices (with different number of pins) of the multi-chip package based on the testing result [lines 31-35 of column 6].

Takizawa does not disclose performing a contact test for all different types of semiconductor devices of the multi-chip package.

Goins, III (hereafter Goins) discloses performing a contact test [using 350, 360 of 300, see Fig. 7] for all different types [e.g. different heights of SIMM or DIMM] of semiconductor devices [all MCM 400] of the multi-chip package and bin sorting once for all different types of semiconductor devices of the multi-chip package based on the testing result [lines 48-51 of column 3]. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the multi-chip package of Takizawa (which discloses multi-chip module formed of multiple type of semiconductor devices) for contact test as taught by Goins at once, since Goins performs automatic handling and testing of MCM to obtain advantage as further disclosed at lines 36-53 of column 2.

10. Claims 11 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa as applied to claim 21 above, and further in view of Goins.

Regarding claims 11 and 25, Takizawa discloses all the elements except for performing a contact test once for all different types of semiconductor devices of the multi-chip package and bin sorting once for all different types of semiconductor devices of the multi-chip package based on the testing result.

Goins discloses performing a contact test [using 350, 360 of 300] for all different types of semiconductor devices [all MCM 400] of the multi-chip package and bin sorting once for all different types of semiconductor devices of the multi-chip package based on the testing result [lines 48-51 of column 3]. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the multi-chip package of Takizawa (which discloses multi-chip module formed of multiple type of semiconductor devices) for contact test as taught by Goins at once, since Goins performs automatic handling and testing of MCM to obtain advantage as further disclosed at lines 36-53 of column 2.

11. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa as applied to claims 1 and 14 respectively above.

Regarding claims 7 and 19, Takizawa discloses all the elements except for multi-chip package is in the form of a TBGA. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-chip package is in the form of a TBGA, since it was known in the art that thin tape as circuit board (to mount multi-chips) has improved thermal reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel
Primary Examiner
Art Unit 2829

May 26, 2005